Amendments to the Claims

The listing of claims below replaces all prior versions and listings of claims.

Listing of Claims

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Claim 1 (Currently Amended): A phase detector, comprising:

a first input that receives a first signal;

a second input that receives a second signal;

a comparison circuit that generates an output signal that is a function of a phase difference between the first signal and the second signal; and

an operating point circuit that maintains an operating point of the phase detector such that for a predetermined range of both positive and negative phase differences between the first and second signals, the output signal is generated as a substantially linear function of the phase difference between the first signal and the second signal, wherein the substantial linearity of the output signal is due at least in part to a shifting of the operating point so that a zero output signal corresponds to a nonzero phase difference between the first and second signals.

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Claim 2 (Currently Amended): The phase detector of claim 1, wherein:

the phase detector is employed in a phase-locked loop, whereby an output frequency of the phase-locked loop is a function of the output signal of the phase detector; and

~~and~~ the operating point circuit leaks a predefined portion of the output signal so as to prevent the leaked output signal from influencing the output frequency of the phase-locked loop.

Claim 3 (Original): The phase detector of claim 1, wherein the output signal is an output current; and wherein the comparison circuit comprises:

a first circuit that asserts a first charge pump control signal in response to an edge of the first signal;

a second circuit that asserts a second charge pump control signal in response to an edge of the second signal;

a first charge pump that contributes a positive current to the output current in response to assertion of the first charge pump control signal;

a second charge pump that contributes a negative current to the output current in response to assertion of the second charge pump control signal; and

reset logic that supplies a reset signal to each of the first and second circuits in response to both of the first and second charge pump control signals being asserted, and

wherein the operating point circuit comprises:

a delay circuit that delays at least one of the first and second charge pump control signals from being supplied to the reset logic, wherein a length of time that it takes the first charge pump control signal to be supplied to the reset logic is not equal to the length of time that it takes the second charge pump control signal to be supplied to the reset logic.

Claim 4 (Original): The phase detector of claim 3, wherein the delay circuit delays only one of the first and second charge pump control signals from being supplied to the reset logic.

Claim 5 (Original): The phase detector of claim 3, wherein the delay circuit delays both the first and second charge pump control signals from being supplied to the reset logic.

Claim 6 (Original): The phase detector of claim 1, wherein the output signal is an output voltage; and wherein the comparison circuit comprises:

a first circuit that asserts a first voltage generator control signal in response to an edge of the first signal;

a second circuit that asserts a second voltage generator control signal in response to an edge of the second signal;

a first voltage generator that contributes a positive voltage to the output voltage in response to assertion of the first voltage generator control signal;

a second voltage generator that contributes a negative voltage to the output voltage in response to assertion of the second voltage generator control signal; and

reset logic that supplies a reset signal to each of the first and second circuits in response to both of the first and second voltage generator control signals being asserted, and

wherein the operating point circuit comprises:

a delay circuit that delays at least one of the first and second voltage generator control signals from being supplied to the reset logic, wherein a length of time that it takes the first voltage generator control signal to be supplied to the reset logic is not equal to the length of time that it takes the second voltage generator control signal to be supplied to the reset logic.

Claim 7 (Original): The phase detector of claim 6, wherein the delay circuit delays only one of the first and second voltage generator control signals from being supplied to the reset logic.

Claim 8 (Original): The phase detector of claim 6, wherein the delay circuit delays both the first and second voltage generator control signals from being supplied to the reset logic.

Claim 9 (Currently Amended): A phase-locked loop comprising:

a phase detector that comprises:

a first input that receives a reference clock signal; a second input that receives a feedback signal; and

a comparison circuit that generates a phase detector output signal that is a function of a phase difference between the reference clock signal and the feedback signal;

an operating point circuit that maintains an operating point of the phase detector such that for a predetermined range of both positive and negative phase differences between the reference clock and feedback signals, the output signal is generated as a substantially linear function of the phase difference between the reference clock and feedback signals, wherein the substantial linearity of the output signal is due at least in part to a shifting of the operating point so that a zero output

signal corresponds to a nonzero phase difference between the reference clock and feedback signals;

a loop filter that generates a frequency control signal from the phase detector output signal;

a circuit that generates a phase-locked loop output signal that has a frequency that is controlled by the frequency control signal;

a frequency divider that generates the feedback signal from the phase-locked loop output signal; and

one or more circuit elements that leak a predefined portion of at least one of the phase detector output signal and the frequency control signal so as to prevent the leaked output signal from influencing the output frequency of the phase-locked loop.

Claim 10 (Original): The phase-locked loop of claim 9, wherein the one or more circuit elements that leak a predefined portion of at least one of the phase detector output signal and the frequency control signal comprise:

one or more circuit elements in the loop filter that leak a predefined portion of the phase detector output signal.

Claim 11. (Original): The phase-locked loop of claim 9, wherein the circuit that generates the phase-locked loop output signal that has a frequency that is controlled by the frequency control signal is a voltage controlled oscillator.

Claim 12 (Original): The phase-locked loop of claim 9, wherein the circuit that generates the phase-locked loop output signal that has a frequency that is controlled by the frequency control signal is a current controlled oscillator.

Claim 13 (Currently Amended): A method of detecting a phase difference between a first signal and a second signal, the method comprising:

generating an output signal that is a function of a phase difference between the first signal and the second signal; and

maintaining an operating point of the phase detector such that for a predetermined range of both positive and negative phase differences between the first and second signals, the output signal is generated as a substantially linear function of the phase difference between the first signal and the second signal, wherein the substantial linearity of the output signal is due at least in part to a shifting of the operating point so that a zero output signal corresponds to a nonzero phase difference between the first and second signals.

Claim 14 (Original): The method of claim 13, further comprising:

generating a phase-locked loop output signal that has a frequency that is a function of the output signal of the phase detector; and

leaking a predefined portion of the output signal so as to prevent the leaked output signal from influencing the output frequency of the phase-locked loop output signal.

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Claim 15 (Original): The method of claim 13, wherein

the output signal is an output current; and

wherein the step of generating the output signal that is a function of the phase difference between the first signal and the second signal comprises:

asserting a first charge pump control signal in response to an edge of the first signal;

asserting a second charge pump control signal in response to an edge of the second signal;

contributing a positive current to the output current in response to assertion of the first charge pump control signal;

contributing a negative current to the output current in response to assertion of the second charge pump control signal; and

deactivating the first and second charge pump control signals in response to both of the first and second charge pump control signals being asserted, and

wherein the step of maintaining the operating point of the phase detector comprises:

delaying at least one of the first and second charge pump control signals from affecting the deactivating step, wherein a length of time that it takes the first charge pump control signal to affect the deactivating step is not equal to the length of time that it takes the second charge pump control signal to affect the deactivating step.

Claim 16 (Original): The method of claim 15, wherein the step of delaying comprises delaying only one of the first and second charge pump control signals from affecting the deactivating step.

Claim 17 (Original): The method of claim 15, wherein the step of delaying comprises delaying both the first and second charge pump control signals from affecting the deactivating step.

Claim 18 (Original): The method of claim 13,

wherein the output signal is an output voltage; and

wherein the step of generating the output signal that is a function of the phase difference between the first signal and the second signal comprises:

asserting a first voltage generator control signal in response to an edge of the first signal;

asserting a second voltage generator control signal in response to an edge of the second signal;

contributing a positive voltage to the output voltage in response to assertion of the first voltage generator control signal;

contributing a negative voltage to the output voltage in response to assertion of the second voltage generator control signal; and

deactivating the first and second voltage generator control signals in response to both of the first and second voltage generator control signals being asserted, and

wherein the step of maintaining the operating point of the phase detector comprises:

delaying at least one of the first and second voltage generator control signals from affecting the deactivating step, wherein a length of time that it takes the first voltage generator control signal to affect the deactivating step is not equal to the

length of time that it takes the second voltage generator control signal to affect the deactivating step.

Claim 19 (Original): The method of claim 18, wherein the step of delaying comprises delaying only one of the first and second voltage generator control signals from affecting the deactivating step.

Claim 20 (Original): The method of claim 18, wherein the step of delaying comprises delaying both the first and second voltage generator control signals from affecting the deactivating step.

Claim 21 (Currently Amended): A method of generating a phase-locked loop output signal, comprising:

generating a phase detector output signal that is a function of a phase difference between a reference clock signal and a feedback signal;

maintaining an operating point of the phase detector such that for a predetermined range of both positive and negative phase differences between the reference clock and feedback signals, the output signal is generated as a substantially linear function of the phase difference between the reference clock and feedback signals, wherein the substantial linearity of the output signal is due at least in part to a shifting of the operating point so that a zero output signal corresponds to a nonzero phase difference between the reference clock and feedback signals;

generating a frequency control signal from the phase detector output signal;

generating the phase-locked loop output signal that has a frequency that is controlled by the frequency control signal;

using a frequency divider to generate the feedback signal from the phase-locked loop output signal; and

leaking a predefined portion of at least one of the phase detector output signal and the frequency control signal so as to prevent the leaked output signal from influencing the output frequency of the phase-locked loop.

Claim 22 (Original): The method of claim 21, wherein the step of leaking a predefined portion of at least one of the phase detector output signal and the frequency control signal comprises:

leaking a predefined portion of the phase detector output signal in a loop filter.